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09/615,646	07/13/2000	Josh Hogan	10990815-1	4699

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Hewlett-Packard Company
Intellectual Property Administration
P O Box 272400
Fort Collins, CO 80528-9599

EXAMINER	
BATTAGLIA, MICHAEL V	
ART UNIT	**PAPER NUMBER**
2652	2

DATE MAILED: 09/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/615,646	HOGAN ET AL.	
	Examiner	Art Unit	
	Michael V Battaglia	2652	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21-26* is/are rejected.

7)☒ Claim(s) *16-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 July 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figures 1-3 should be designated by a legend such as –Prior Art– because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informality. On page 1, line 11, the examiner suggests inserting -data- after "new". Appropriate correction is required.

Claim Objections

3. Claim 16 is objected to because of the following informalities:

a. On line 1, the examiner suggests removing the second "block".

b. On line 10, the examiner suggests inserting -header- after "actual".

Appropriate correction is required.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5-9, 14-18, 21, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Kobayashi et al (US 5,835,461).

In regard to claim 1, Kobayashi et al discloses a method of reading a block of data stored on an optical disc, the data block including header information (Col. 11, lines 48-50), the method comprising the steps of synthesizing header information for the data block by producing synchronization and address information from the wobbling signal (Col. 8, lines 41-64); recovering actual header information from the disc (Col. 8, lines 34-40); and recovering actual user data from the disc (Col. 8, lines 14-17), the user data being phase shifted by a phase difference between the synthesized and recovered header information. The user data is phase shifted by the phase-adjusted clock produced by the VCO, which is a read/write clock used for recording/reproduction when supplied to the recording/reproduction circuit (Col. 8, line 65 - Col. 9, line 13).

In regard to claim 2, Kobayashi et al discloses that the step of synthesizing the header information includes the steps of recovering address information from a wobble embossed on the disc (Col. 8, lines 41-64); and synthesizing the header information from the recovered address information (Col. 9, lines 12-20).

In regard to claim 3, Kobayashi et al discloses that the step of synthesizing the header information includes the steps of obtaining address information from the disc (Col. 8, lines 41-64); and synthesizing the header information from the obtained address information (Col. 9, lines 12-20).

In regard to claim 5, Kobayashi et al discloses that the header information is synthesized by modulation encoding the address information according to a pre-specified format (Col. 6, lines 50-52).

In regard to claims 6 and 7, Kobayashi et al discloses that the synthesized header information includes a sector address and an error detection code (Col. 6, lines 19-33).

In regard to claim 8, Kobayashi et al discloses that a combination of analog and digital techniques are used to phase-shift the recovered user data, wherein the voltage controlled oscillator in the PLL circuit (Fig. 14, element 44 in element 41) constitutes the analog technique and the sector counter constitutes the digital technique (Fig. 14, element 46).

In regard to claim 9, Kobayashi et al discloses that a read clock is used to recover the data; and wherein the recovered data is phase shifted by creating a phase difference between the read clock and the recovered user data (Col. 8, line 65 - Col. 9, line 13).

In regard to claim 14, Kobayashi et al discloses a read clock for recovering the block from the disc; and wherein the phase difference is inherently faded towards zero according to a time constant related to the read clock (Col. 8, line 65 - Col. 9, line 13). The phase of clock signal produced by the PLL circuit cannot be instantaneously changed to compensate for a phase difference between the output of the mark detection circuit and the output of the divider. Therefor, the compensation occurs gradually as the phase difference is faded to zero.

In regard to claim 15, Kobayashi et al discloses a bit-accurate read/write drive for reading a data block from a disc, the drive comprising means for synthesizing header information for the data block (Fig. 14, elements 36-37, 40, and 46); means for recovering actual header information from the disc (Fig. 14, elements 32-33 and 35); and means for recovering actual user data from the disc, the user data being phase-shifted by a phase difference between the synthesized and actual

header information (Fig. 14, elements 32-33 and 41). The examiner notes that drive is interpreted to mean a device that reads data from and/or writes data onto a storage medium.

In regard to claim 16, Kobayashi et al discloses an apparatus for reading a block of data block from an optical disc, the apparatus comprising an optical pickup unit (Figure 14, element 32); an address detector (Figure 14, elements 33-34); a data recovery circuit for recovering data from an output of the optical pickup unit, the recovered data including actual header information and actual user data of the data block (Figure 14, element 33); a first circuit for synthesizing header information for the data block (Fig. 14, elements 36-37, 40, and 46); a second circuit for determining a phase difference between the recovered actual and synthesized header information (Fig. 14, element 41); and a third circuit for phase-shifting the recovered user data by the determined phase difference (Figure 14, element 33).

In regard to claim 17, Kobayashi et al discloses that the first circuit synthesizes the header information by recovering address information from a wobble embossed on the disc and synthesizing the header information from the recovered address information (Fig. 14, elements 35-36 and 40 and Col. 8, lines 44-51).

In regard to claim 18, Kobayashi et al discloses that address information is contained on the disc; and wherein the first circuit synthesizes the header information from the address information contained on the disc (Fig. 14, elements 35-36 and 40 and Col. 8, lines 44-51).

In regard to claim 21, Kobayashi et al discloses that the data recovery circuit includes a read clock (Figure 14, element CLOCK and Col. 9, lines 12-13) and wherein the recovered actual data is phase-shifted by creating a phase difference between the read clock and the recovered actual user data (Col. 8, line 65 - Col. 9, line 11).

In regard to claim 26, Kobayashi et al discloses an apparatus for correcting a signal recovered during a read operation on a data block stored on a disc, the recovered signal including actual header information and actual user data of the data block (Col. 8, lines 34-40), the apparatus comprising a first circuit for synthesizing header information for the data block (Fig. 14, elements 36-37, 40, and 46); a second circuit for determining a phase difference between the recovered and synthesized header information (Fig. 14, element 41); and a third circuit for phase-shifting the recovered user data by the determined phase difference (Figure 14, element 33).

5. Claims 16 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Kobayashi (US 6,373,816).

In regard to claim 16, Kobayashi discloses an apparatus for reading a block of data block from an optical disc, the apparatus comprising an optical pickup unit (Figures 5 and 8, element 11); an address detector (Figures 5 and 8, elements 37); a data recovery circuit for recovering data from an output of the optical pickup unit, the recovered data including actual header information and actual user data of the data block (Figure 8, element 53); a first circuit for synthesizing header information for the data block (Fig. 5, elements 39-40); a second circuit for determining a phase difference between the recovered actual and synthesized header information (Fig. 5, element 35); and a third circuit for phase-shifting the recovered user data by the determined phase difference (Figure 8, element 53).

In regard to claim 25, Kobayashi discloses that the apparatus is a DVD drive (Col. 1, lines 25-35).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al in view of Honma (US 5,917,794).

Kobayashi et al discloses the method and apparatus for reading a block of data from an optical disc wherein header information is synthesized from address information obtained on the disc by a first circuit as claimed in claims 1, 3, 16, and 18. Kobayashi et al does not disclose that multiple candidates are synthesized from the address information by a second circuit; wherein a phase difference between the actual header information and a best candidate is determined; and wherein the recovered user data is shifted according to the determined phase difference. The examiner notes that Kobayashi et al disclose using a disc that contains header information, address information, and user data (Fig. 7 and 17).

Honma discloses a method and apparatus for reading a block of data stored on an optical disc comprising synthesizing information for a data block by a first circuit (Fig. 4, element 42 and Fig. 5, element 42-1), recovering actual information from the disc by a data recovery circuit (the output of the data recovery circuit is shown by Fig. 4, element x), determining a phase difference between the recovered information and the synthesized information by a second circuit (Fig. 4, element 42), the data being phase-shifted by a phase difference between the synthesized and recovered information by a third circuit (Fig. 4, element 44). The examiner notes that the method

and apparatus of Honma would synthesize header information from a data block on the disc of Kobayashi et al because all of the information read from the disc, which would include header information, is synthesized. Honma further discloses synthesizing multiple candidates from the information, which would include address information contained on the disc of Kobayashi et al; wherein a phase difference between the actual information, which would include header information contained on the disc of Koabyashi et al, and a best candidate is determined by the second circuit (Col. 5, lines 14-17 and 41-61); and wherein the recovered information, which would include user data contained on the disc of Kobayashi et al, is shifted according to the determined phase difference (Col. 5, lines 27-35). In addition, Honma teaches that use of maximum likelihood detectors that select a best candidate from multiple candidates will lead to lead to a lower error rate of information detection (Col. 1, lines 26-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to synthesize multiple candidates from the address information recovered from the disc in the method and apparatus of Kobayashi et al and to shift the recovered user data according to the phase difference between the actual information, including header information, and a best candidate as taught by Honma; the motivation being to detect information on a disc with a low error rate.

7. Claims 10 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al in view of Honma.

Kobayashi et al discloses the method and apparatus for reading a block of data from an optical disc wherein a read clock is used to recover the data; and wherein the recovered data is phase shifted by creating a phase difference between the read clock and the recovered user data as

claimed in claims 1, 9, 16, and 21. Kobayashi et al does not disclose that the recovered data is phase shifted by time-delaying the recovered data.

Honma discloses a method and apparatus for reading a block of data stored on an optical disc comprising synthesizing information for a data block by a first circuit (Fig. 4, element 42 and Fig. 5, element 42-1), recovering actual information from the disc by a data recovery circuit (the output of the data recovery circuit is shown by Fig. 4, element x), determining a phase difference between the recovered information and the synthesized information by a second circuit (Fig. 4, element 42), the data being phase-shifted by a phase difference between the synthesized and recovered information by a third circuit (Fig. 4, element 44). The examiner notes that the method and apparatus of Honma would synthesize header information from a data block on the disc of Kobayashi et al because all of the information read from the disc, which would include header information, is synthesized. Honma further discloses that recovered data is phase shifted by time-delaying the recovered data (Col. 5, lines 27-35) and teaches that by time-delaying the recovered data, the amplitude of fluctuation can be detected (Col. 5, lines 24-27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to phase shift the recovered data in the method and apparatus of Kobayashi et al by time-delaying the recovered data as taught by Honma; the motivation being to allow for detection fluctuation amplitude.

8. Claims 11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al in view of Horigome (US 5,682,374).

Kobayashi et al discloses the method and apparatus for reading a block of data from an optical disc wherein a read clock is used to recover the data; and wherein the recovered data is phase shifted by creating a phase difference between the read clock and the recovered user data as

claimed in claims 1, 9, 16, and 21. Kobayashi et al does not disclose that the recovered data is phase shifted by time-delaying the read clock.

Horigome discloses a method and apparatus for reading a block of data from an optical disc wherein a read clock is used to recover the data; and wherein the recovered data is phase shifted by creating a phase difference between the read clock and the recovered user data (Fig. 11 and Col. 16, lines 54-58). Horigome further discloses a phase adjustment circuit (Fig. 11, element 44) that comprises delay circuits (Fig. 11, elements 51 and 61) for time-delaying the read clock (Fig. 11, SMPLCLK) to shift the phase of the recovered user data. Horigome teaches adjusting the phase of the read clock to allow for reproduction from a higher density recording.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to time-delay the read clock in the method and apparatus of Kobayashi et al to phase shift the recovered data as suggested by Horigome; the motivation being to reproduce data from a high density recording.

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al in view of Tanoue et al (hereafter Tanoue) (US 6,091,688).

Kobayashi et al discloses a method for reading a block of data from an optical disc as claimed in claim 1. Kobayashi et al does not disclose that the recovered user data is stored in memory prior to demodulation; and wherein the recovered user data is digitally phase-shifted by shifting the data stored in the memory.

Tanaoue discloses a method for reading a block of data from an optical disc, wherein actual header information and user data are recovered form the disc. Tanoue further discloses that the recovered user data is stored in memory prior to demodulation; and wherein the recovered user data is digitally phase-shifted by shifting the data stored in the memory (Fig. 15,

elements 74 and 75). The examiner notes that the data stored in the memory of Tanoue will inherently be digitally phase-shifted because the memory is a shift register. Tanoue teaches that storing the data in memory will allow the serial data to be converted to parallel data to be operated on by the demodulation circuit (Col. 16, lines 48-52).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to store user data from the circuit of Kobayashi et al in memory prior to demodulation and to digitally phase shift recovered user data in the memory; the motivation being to convert the recovered user data to parallel data to be operated on by the demodulation circuit.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al in view of Tsuyoshi et al (hereafter Tsuyoshi) (US 4,748,611).

Kobayashi et al discloses the method for reading a block of data from an optical disc as claimed in claim 1. Kobayashi et al does not disclose that a phase difference between synthesized and recovered header information is determined for only the first data sector of the block.

Tsuyoshi discloses a method for reading a block of data from an optical disc wherein a phase difference is determined for only the first data sector of the block (Fig. 5A and Col. 8, lines 8-21) and teaches that having header information, including address and synchronization information only at the beginning of each data block will raise data capacity of the disc (Fig. 5A and Col. 3, line 68-Col. 4, line 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to determine a phase difference between synthesized and recovered header information in the method of Kobayashi et al for only the first data sector of the block as suggested by Tsuyoshi; the motivation being to raise the data capacity of the disc.

11. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al in view of Tsuyoshi.

Kobayashi et al discloses the apparatus for reading a block of data from an optical disc as claimed in claim 16. Kobayashi et al further discloses a read clock used by the data recovery unit; and wherein the phase difference is inherently faded towards zero according to a time constant related to the read clock by the second circuit (Col. 8, line 65 - Col. 9, line 13). The examiner notes that the phase of clock signal produced by the PLL circuit cannot be instantaneously changed to compensate for a phase difference between the output of the mark detection circuit and the output of the divider. Therefor, the compensation occurs gradually as the phase difference is faded to zero. Kobayashi et al does not disclose that the second circuit determines a phase difference only for the first data sector of the block.

Tsuyoshi discloses a method for reading a block of data from an optical disc wherein a phase difference is determined for only the first data sector of the block (Fig. 5A and Col. 8, lines 8-21) and teaches that having header information, including address and synchronization information only at the beginning of each data block will raise data capacity of the disc (Fig. 5A and Col. 3, line 68-Col. 4, line 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the second circuit of Kobayashi et al to determine a phase difference between synthesized and recovered header information for only the first data sector of the block as suggested by Tsuyoshi and then to fade the phase difference to zero according to a time constant related to the read clock; the motivation being to raise the data capacity of the disc.

Citation of Relevant Prior Art

Ogino et al (US 4,740,942) discloses a variable delay unit and a shift register memory (Fig. 4, elements 10 and 18-19). Winslow et al (US 4,353,089) discloses a variable delay memory device (Fig. 1, element 89). Zwaans (US 5,043,966) discloses a shift register (Fig. 1, element 2) wherein data is read in at a variable frequency and read out at a constant frequency. Yokogawa et al (US 5,440,532) discloses using an interpolator circuit (Fig. 10, element 24) for synthesizing a best candidate.

Allowable Subject Matter

12. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

None of the references alone or in combination disclose or suggest a circuit for phase shifting recovered user data by a phase difference between recovered and synthesized header information comprising a variable delay for shifting by a fractional portion of the phase difference and memory for shifting by an integer portion of the phase difference.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael V Battaglia whose telephone number is (703) 305-4534. The examiner can normally be reached on 5-4/9 Plan with 1st Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa T Nguyen can be reached on (703) 305-9687. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Michael Battaglia

HOA T. NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600
9/8/03